Patent claims

1. A semiconductor device having a semiconductor chip stack (1) on a rewiring plate (2),
   - the underside (3) of the rewiring plate (2) forming the underside (3) of the semiconductor device (4),
   - an external contact area (5) having a plurality of external contact area regions (6 to 9) which are physically separate from one another being arranged on the underside (3),
   - the individual external contact area regions (6 to 9) being assigned to the individual semiconductor chips (10 to 13) in the semiconductor chip stack (1), and
   - the regions (6 to 9) of an individual external contact area (5) being electrically connected via a common external contact (14).

2. The semiconductor device as claimed in claim 1, characterized in that
the rewiring plate (2) comprises, on its top side (25), a rewiring structure (15) which comprises, in the center (19) of the rewiring plate (2), contact pads (16) for connecting a semiconductor chip (10) to flip-chip contacts (18) and comprises, in the edge region (17), contact pads (20) for bonding connections to a stacked semiconductor chip (11, 12, 13).

3. The semiconductor device as claimed in claim 1 or claim 2,
characterized in that
the rewiring plate (2) comprises, in the center (19) of its top side (25), a rewiring structure (15) for fitting the rear side (22) of a lower semiconductor chip (11) and comprises, in the edge

regions, contact pads (20) for bonding connections (21) to top sides (23) of the stacked semiconductor chips (12, 13, 14).

4. The semiconductor device as claimed in one of the preceding claims,
characterized in that
the rewiring plate (2) comprises through-contacts (24) via which the contact pads (16, 20) on the top side (25) of the rewiring plate (2) are connected to the external contact area regions (7 to 9) on the underside (3) of the rewiring plate (2).

5. The semiconductor device as claimed in one of the preceding claims,
characterized in that
the rewiring plate (2) comprises rewiring lines (26) which connect the external contact area regions (6 to 9) to the contact pads (16, 20).

6. The semiconductor device as claimed in one of the preceding claims,
characterized in that
the semiconductor chips (11 to 13) of the semiconductor device (4) comprise, on their active top sides (23), contact areas (27) which are connected, via flip-chip contacts (18) and/or bonding connections (21), to the contact pads (16, 20) on the top side (25) of the rewiring plate (2).

7. The semiconductor device as claimed in one of the preceding claims,
characterized in that
the semiconductor chip stack (1) on the rewiring plate (2) is embedded in a plastic composition (28).

8. A panel which comprises device positions which are arranged in rows and columns and have semiconductor devices (4) as claimed in one of claims 1 to 7.

9. A method for producing and testing a panel having semiconductor device positions which are arranged in rows and columns and have semiconductor chip stacks (1), the method comprising the following method steps:

- producing a circuit carrier in the form of a rewiring plate (2) having rewiring lines (26) which electrically connect, via through-contacts (24), contact pads (16, 20) on the top side (25) of the circuit carrier to external contact area regions (6 to 9) on the underside (3) of the circuit carrier, the external contact area regions (6 to 9) being patterned in such a manner that a plurality of external contact area regions (6 to 9) are provided for the purpose of fitting an external contact (14);
- applying a stack (1) of semiconductor chips (10 to 13) to the circuit carrier with connection of contact areas (27) of the semiconductor chips (10 to 13) to contact pads (16, 20) on the top side (25) of the circuit carrier;
- covering the circuit carrier with a plastic composition (28) in the region of the semiconductor device positions;
- testing each individual semiconductor chip (10 to 13) in a semiconductor chip stack (1) using the corresponding external contact area regions (6 to 9) on the underside (3) of the circuit carrier;
- marking defective semiconductor devices (10 to 13).

10. A method for producing semiconductor devices (4) having semiconductor chip stacks (1), said method having the following method steps of:

- producing a panel as claimed in claim 9;
- applying external contacts (14) to the external contact area regions (6 to 9) with electrical connection of the external contact area regions (6 to 9);
- separating the panel into individual semiconductor devices (4).